



ECIT

The Institute of Electronics,
Communications and
Information Technology



Queen's University
Belfast

The Institute of Electronics, Communications and Information Technology (ECIT) is a new £40M research centre that brings together in one building Queen's University Belfast's internationally renowned expertise in electronics and computer science. ECIT is located off-campus on the Northern Ireland Science Park.

Its mission is to stimulate major opportunities for economic growth, by pioneering future directions and innovation in key areas of advanced technology. It does this through a healthy mixture of speculative blue skies, applied and strategic research.

The Institute extends the significant links Queen's University has with major high technology companies, universities and research centres throughout the world. It also provides "hot-housing" facilities to encourage and support the growth of new spin-off and spin-in companies.



System-on-Chip (SoC) Research

The SoC research division is comprised of over 35 academic and research/research-related support staff. The division's research aspiration is to challenge the widening technology and data processing gaps that exist for emerging and future services and applications of converging information and communication technologies.

Research targets:

- » Novel SoC architectures
- » High-level SoC design methodologies
- » Programmability of systems

A key aspect is to meet the real-time computational and flexibility demands of converging systems.

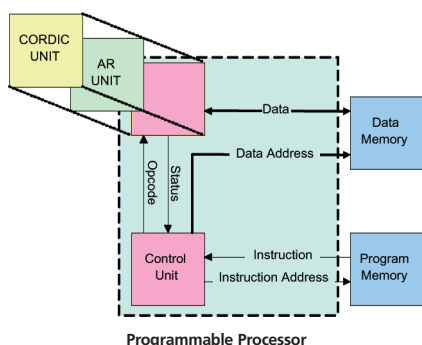
Current SoC research includes:

- » Communication Signal and Video Processing
- » Cryptography
- » Image and Video Analysis Systems
- » Network Processing
- » Network Security Processing
- » Programmable Systems
- » Wireless Communication Systems

SoC Architectures

Research in SoC Architectures targets the derivation of novel and efficient platform-architectures for networks, communication and video signal processing systems that are computationally intensive.

Previous research has shown how complex functions such as MPEG2, MPEG4, JPEG2000 compression algorithms, frame/packet processing and configurable cryptographic algorithms can be created hierarchically using a library of lower level architectural templates or sub-function blocks. Such an approach allows not only reuse of but also the rapid development and deployment of assessable trade-offs for complex architectures and systems. Current research investigates the decomposition of complex functions, and explores architectural limitations and scalability issues. These are then used to derive novel heterogeneous SoC architectures that allow the best trade-off for a spectrum of applications in terms of performance, power consumption, cost and flexibility.



Current projects include heterogeneous video and signal processing architectures, programmable processor architectures for communications signal processing applications (such as adaptive beamforming and MIMO systems for wireless communications), and low-power hardware design for high-end DSP systems.

Contact: Dr Sakir Sezer
Professor John McCanny

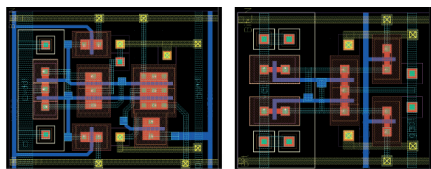
Email: S.Sezer@qub.ac.uk

Cryptography

Research in Cryptography involves the development of SoC architectures for applications and systems that require acceleration in processing cryptographic algorithms. High-speed cryptographic architectures of the AES, SHACAL-2, Whirlpool, RSA and ECC algorithms have been realised. Other research projects currently being undertaken include the design of generic microprocessor architectures for cryptography, wireless ad-hoc network security protocols and architectures, network security processing and cryptographic architectures for constrained environments.

Contact: Dr Maire McLoone

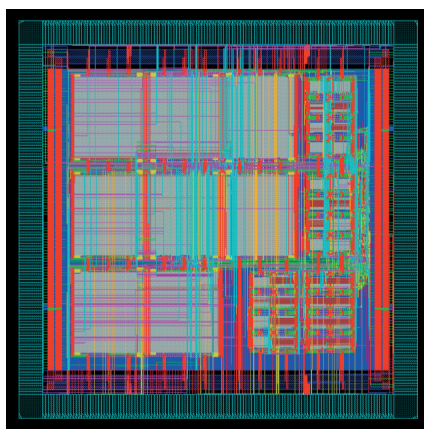
Email: M.McLoone@ecit.qub.ac.uk



Full custom CAM/RAM cells

Network Processing

Research in Network Processing is challenging the widening technology and network processing gap that exists between demands on network processing at network nodes and access equipment. The research primarily targets hardware-based and domain-specific network processing architectures for line rates between 10 and 1000 Gbps. Current research activities encompass highly scalable QoS traffic management processing architectures, adaptive and QoS aware scheduling algorithms and architectures (especially mobile and fixed-wireless networks), heterogeneous packet/frame processing architectures, trade-offs of embedded memory architectures and technologies for network processing, and MAC algorithms and processing architectures for SDMA and MIMO-based wireless communication systems.



WFQ packet scheduler for 40 Gbps line rate

Contact: Dr Sakir Sezer

Email: S.Sezer@qub.ac.uk

Programmable Systems

Research in programmable systems is focused mainly around the use of programmability of technology, in the form of FPGAs, DSPs and embedded processors, for a range of applications and systems where programmability is a distinct feature. Furthermore, the programmability of SoC architectures in the form of a configurable datapath, ASIPs and embedded configurable logics for high-performance communication signal processing, video compression, cryptography and network processing are investigated. Achievements include the development of a synthesis flow from dataflow graph (DFG) descriptions onto heterogeneous systems incorporating multiple processors and FPGAs. This enables users to explore hardware optimisations at the DFG level, resulting in considerable performance improvements and leading to new ways of developing silicon IP cores.

Contact: Dr John McAllister
Professor Roger Woods

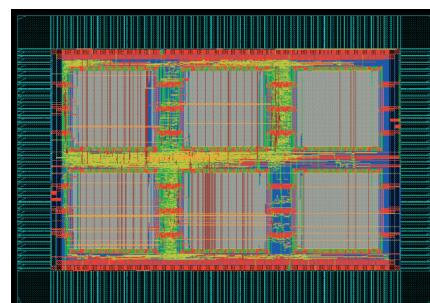
Email: J.McAllister@ecit.qub.ac.uk

Network Security Processing

Emerging stream-based Internet services and e-businesses require significantly more bandwidth and improved security measures. These new measures depend upon extensive and complex security processing capabilities to protect users, e-businesses, online services and networks. The prevention of illegitimate access to private content or personal information, unauthorized access to services, applications and networks, and the protection from unwanted and unlawful content (spam) requires customised and hardware accelerated content processing. Research undertaken explores accelerated packet classification, hardware-based parallel deep packet inspection (DPI) and hardware accelerated IP Security (IPSec) processing.

Contact: Dr Sakir Sezer
Dr Maire McLoone

Email: S.Sezer@qub.ac.uk



Associative Memory

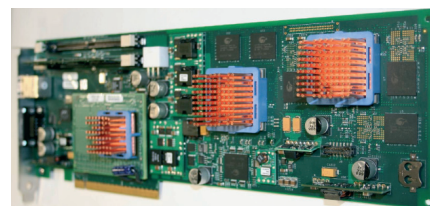
Speech, Image & Video Processing and Analysis Systems

Research in speech, image and video processing and analysis systems targets heterogeneous system architectures for accelerated speech recognition and image and video analysis. Algorithmic complexity to meet user expectations for naturalness and robustness in speech driven interfaces exceeds the processing and power capabilities of many embedded processor technologies. New architectures are therefore needed to accelerate state-of-the-art recognition technology for mobile and embedded devices.

Emerging video analysis systems for security, broadcast media and scientific and medical imaging applications require significant acceleration in hardware to enable processing throughput to meet the real-time expectations of target applications. Novel architectures for complex analysis algorithms are targeted to our ipaX platform to satisfy high processing and high memory bandwidth performance requirements.

Contact: Laurent Wojcieszak
Dr Paul McCourt

Email: L.Wojcieszak@ecit.qub.ac.uk



ipaX Board for Image and Video Analysis